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High-performance sub-10-nm monolayer black phosphorene tunneling transistors

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ABSTRACT

Moore's law is approaching its physical limit. Tunneling field-effect transistors (TFETs) based on 2D materials provide a possible scheme to extend Moore's law down to the sub-10-nm region owing to the electrostatic integrity and absence of dangling bonds in 2D materials. We report an *ab initio* quantum transport study on the device performance of monolayer (ML) black phosphorene (BP) TFETs in the sub-10-nm scale (6–10 nm). Under the optimal schemes, the ML BP TFETs show excellent device performance along the armchair transport direction. The on-state current, delay time, and power dissipation of the optimal sub-10-nm ML BP TFETs significantly surpass the latest International Technology Roadmap for Semiconductors (ITRS) requirements for high-performance devices. The subthreshold swings are 56–100 mV/dec, which are much lower than those of their Schottky barrier and metal oxide semiconductor field-effect transistor counterparts.

1 Introduction

Lowering the power consumption while maintaining high on-state current (I_{on}) is one of the imperative pursuits for next-generation field-effect transistors (FETs) during the on-going scale-down effort. Tunneling field-effect transistors (TFETs) provide a possible scheme to lower the power consumption because they have the ability to further reduce the subthreshold swing (SS) to sub-60-mV/dec, which is the thermal diffusion limit of conventional metal–oxide–semiconductor FETs (MOSFETs) and Schottky barrier FETs (SBFETs). In 1978, TFETs based on planar p-i-n structure were first proposed by Quinn et al. [1]. To date, TFETs with SS < 60 mV/dec are fabricated using bulk silicon, germanium, and III–IV materials down to the scale of several tens of nanometers, in experiments using this p-i-n geometry [2–4]. However, in these

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three-dimensional (3D) TFETs, low SS (< 60 mV/dec) is only effective at currents of 10^{-8}–10^{-3} μA/μm [3, 4], and the corresponding I_{on} is generally too small with values of 10^{-6}–10^{-1} μA/μm [3, 4], which limits their practical application. Two-dimensional (2D) semiconducting materials provide an opportunity to break the limitation of low I_{on} owing to their natural atomic thin layer and clean surface [4–10]. The atomic thin body allows excellent gate control; moreover, the clean surface has few traps on the semiconductor–dielectric interface to block the carrier transport. Both these factors are beneficial for high on-state current.

Since its discovery in 2014, 2D black phosphorene (BP) has attracted wide attention owing to its anisotropic electronic property, moderate and tunable direct band gap, and high carrier mobility [11–13]. Monolayer (ML) and bilayer (BL) BP TFETs in the 10–25 nm scale [14, 15] have been studied using a semi-empirical method, and sharp SS less than 60 mV/dec and much larger I_{on} (1–10^2 μA/μm) than that of bulk TFETs (10^{-6}–10^{-1} μA/μm) have been obtained in ML BP TFETs. The International Technology Roadmap for Semiconductors (ITRS) requires a transistor with a channel less than 10 nm in the next decade. However, the device performance for ML BP TFETs in the sub-10-nm scale is still unknown. It is highly desirable to know whether sub-10-nm ML BP TFETs can satisfy the ITRS requirements, especially in light of the recent experimental breakthrough of sub-10-nm 2D SBFETs based on ML MoS_2 [16–19].

In this paper, we study the device performance of the sub-10-nm ML BP TFETs by using rigorous *ab initio* quantum transport calculations. The intrinsic transfer characteristic and switching ability are carefully examined for the gate length of 6–10 nm. The device performance strongly depends on the transport directions and doping concentration. Under the optimal schemes, the on-state current (1.5×10^3–2.6×10^3 μA/μm), delay time (0.025–0.032 ps), and power dissipation (0.030–0.052 fJ/μm) all exceed the ITRS requirements for the next decade high-performance (HP) transistors. Moreover, we obtain much lower SS (56–100 mV/dec) than those of the ML BP MOSFETs and SBFETs.

2 Models and methods

We choose the armchair direction of ML BP as the transport direction because the current along the armchair direction is eight orders of magnitude larger than that in the zigzag direction for ML BP TFET, according to the previous semi-empirical calculations [14, 15]. The small transport mass along the armchair direction is responsible for the larger source-to-drain tunneling current. We build a double-gated (DG) two-probe TFET model, as illustrated in Fig. 1(a). In the ML BP TFET models, the work functions of the source and drain regions are set to the valence and conduction bands using high p- and n-doping, respectively. Thus, carriers are transported from source to drain through band-to-band tunneling (BTBT) under proper bias, and the on- and off-states can be switched via the band bending of the intrinsic region by gate voltage. The gate lengths of these devices are considered as L_g = 6.17–9.70 nm, with the equivalent oxide thickness (EOT), drain voltage (V_{ds}), and supply voltage (V_{dd}) of each device adapted from the ITRS requirements for HP transistors (2013 version).

The transport properties are calculated using density functional theory (DFT) coupled with nonequilibrium Green's function (NEGF) method, which are implemented in Atomistix ToolKit 2016 package [20–22]. The Monkhorst–Pack k-point mesh [23] of 29 × 1 × 200 is sampled with a k_x separation of approximately 0.01 $Å^{-1}$ along a surface-parallel direction (orthogonal to the transmission direction) in the irreducible Brillouin zone (IBZ) for the electronic self-consistent calculations. The transmission coefficient $T(E, k_x)$ for a given k_x and energy E is obtained as

$$T(E,k_x)=Tr[G^{r}(E,k_x)\cdot\Gamma_S(E,k_x)\cdot G^{a}(E,k_x)\cdot\Gamma_D(E,k_x)]$$

where $G^{r/a}(E, k_x)$ is the retarded/advanced Green's function, and $\Gamma_{S/D}(E,k_x)=i\left(\sum_{S/D}^{r}(E,k_x)-\sum_{S/D}^{a}(E,k_x)\right)$ represents the level broadening owing to the left and right electrodes expressed in terms of the electrode self-energies $\sum_{S/D}^{r/a}(E,k_x)$, which reflects the influence of the electrodes on the scattering region [24]. The transmission function for a given energy $T(E)$ is averaged over different k_x (we considered k_x = 57) in the IBZ. We calculate the current for a given gate voltage V_g and bias voltage V_{ds} by using the Landauer–Büttiker formula [25]

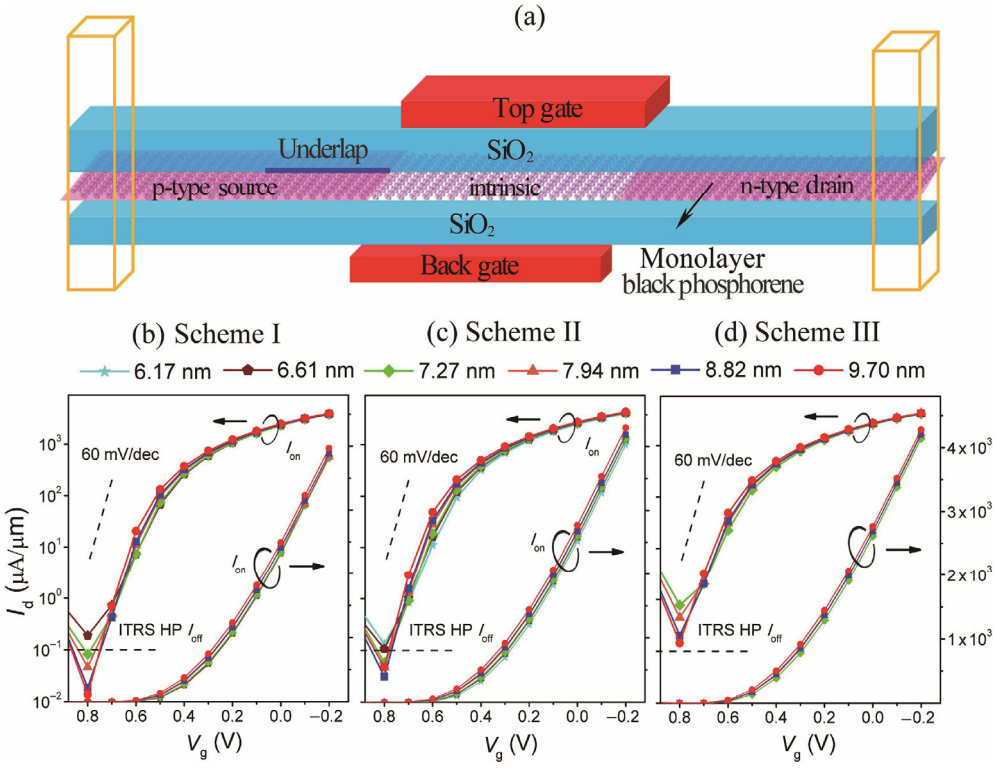

Figure 1 (a) Schematic view of the DG TFET based on ML BP along the armchair transport direction. (b)–(d) Transfer characteristics for the sub-10-nm ML BP DG TFETs along the armchair transport direction under the three schemes at the *ab initio* level. The bias and applied voltages are set according to the ITRS HP requirements.

$$I(V_{ds}, V_g) = \frac{2e}{h}\int_{-\infty}^{+\infty}\{T(E, V_{ds}, V_g)[f_L(E-\mu_L) - f_R(E-\mu_R)]\}dE$$

where $T(E, V_{ds}, V_g)$ is the transmission coefficient, $f_{L/R}$ is the Fermi-Dirac distribution function for the L/R electrode, and μ_L/μ_R is the electrochemical potential of the L/R electrode.

A single-ζ plus polarization basis set is employed, and a test based on the higher accuracy of the double-ζ plus polarization basis set exhibits consistent results (Fig. S1 in the Electronic Supplementary Material (ESM)). The density mesh cutoff is set to 100 Ha, and the temperature is set to 300 K. The generalized gradient approximation (GGA) of Perdew–Burke–Ernzerh form [26] exchange-correlation functional is used. GGA is a good approximation for the transport calculation because many body effects have been significantly depressed in the FET configuration owing to the screening of the electron–electron interaction by doped carriers [27, 28]. For example, the calculated transport gaps of ML, BL, and trilayer (TL) BP SBFETs at the DFT-GGA level are 1.11, 0.81, and 0.66 eV [29–31], respectively, whereas the corresponding measured transport gaps are 1.00, 0.71, and 0.61 eV [11], respectively. The reliability of our method is validated by the general consistency between the simulated and experimental transfer characteristics for the MoS_2 FET with 1-nm-long gate as given in Fig. S2 in the ESM. In particular, the calculated SS is 66 mV/dec, which is approximately equal to the experimental value of 65 mV/dec. The simulated on-state current is one order of magnitude larger than the experimental one. This discrepancy is ascribed to the fact that the MOSFET model is adopted in our simulation with ideal ballistic transport and Ohmic contact features, whereas the experimental MoS_2 FET has a long channel and metal electrode, which result in scattering effect and Schottky barrier, respectively.

3 Results and discussions

We first test the effects of source/drain doping levels (N_s/N_d) and underlap region (UL, intrinsic region not

biased or gated) on the device performance of the DG ML BP TFET with 9.7-nm-long gate, as these two factors are supposed to strongly affect the device performance of ML BP TFETs according to the previous semi-empirical calculation [14]. As shown in Fig. S3 in the ESM, a drastic reduction of the leakage currents is observed when the high drain doping level is maintained and the source doping level is reduced while the on-state currents are maintained at a high level. A similar effect is observed by adding a source underlap. We determine two optimal schemes after the test: Scheme I with N_s = 3 × 10^{12} cm^{-2}, N_d = −5 × 10^{13} cm^{-2}, and UL = 0.0 nm; Scheme II with N_s = 1 × 10^{13} cm^{-2}, N_d = −5 × 10^{13} cm^{-2}, and UL = 4.85 nm. The results of an unoptimized scheme (Scheme III) (N_s = 1 × 10^{13} cm^{-2}, N_d = −5 × 10^{13} cm^{-2}, and UL = 0.0 nm) are also provided for the sake of comparison. With these asymmetric doping concentrations, bipolar character with enhanced p-type characters is detected for all the investigated DG ML BP TFETs, whereas enhanced n-type TFETs with comparable device performance can be easily achieved by simply switching the source and drain doping concentrations (Fig. S4 in the ESM).

Herein, we focus on the enhanced p-type region and plot the transfer characteristics of the DG ML BP TFETs with different gate lengths under the three schemes in Figs. 1(b)–1(d), and the key figures of merit are given in Table 1. Very high maximum currents I_{max} (not on-state current, but the largest current) up to 3.8 × 10^3–4.3 × 10^3 μA/μm are obtained in the three schemes at V_g = −0.2 V. I_{max} (4.3 × 10^3 μA/μm) of our ML BP TFET with 10-nm-long gate is more than one and four orders of magnitude larger than those of the thin (10-nm-thick) Ge/GaAs [32] (approximately 100 μA/μm) and Si/SiGe [33] (approximately 0.2 μA/μm) TFETs with the same gate length at the semi-empirical level, respectively. This is attributed to the atomic thin layer and clean surface, moderate direct band gap (0.9 eV), and anisotropic electronic property of ML BP. The minimum leakage

Table 1 Benchmark of the ballistic device performances of the ML black phosphorene DG TFET against the ITRS requirements for HP transistors of the next decades (2013 version). EOT: equivalent oxide thickness; V_{dd}: supply voltage; SS: subthreshold swing; C_g: intrinsic gate capacitance; τ: delay time; PDP: power dissipation. Scheme I: N_s = 3 × 10^{12} cm^{-2}, N_d = −5 × 10^{13} cm^{-2}, and UL = 0.0 nm; Scheme II: N_s = 1 × 10^{13} cm^{-2}, N_d = −5 × 10^{13} cm^{-2}, and UL = 4.85 nm; Scheme III: N_s = 1 × 10^{13} cm^{-2}, N_d = −5 × 10^{13} cm^{-2}, and UL = 0.0 nm. N_s and N_d represent the source and drain doping concentrations, respectively. UL represents a source underlap.

	L_g (nm)	EOT (nm)	V_{dd} (V)	I_{off} (μA/μm)	I_{on} (μA/μm)	I_{on}/I_{off}	SS (mV/dec)	C_g (fF/μm)	τ (ps)	PDP (fJ/μm)
Scheme I	9.70	0.56	0.74	0.1	2,422	2.42 × 10^4	58.4	0.081	0.025	0.050
Scheme II	9.70	0.56	0.74	0.1	2,480	2.48 × 10^4	56.1	0.106	0.032	0.051
Scheme III	9.70	0.56	0.74	0.145	2,341	1.61 × 10^4	74.2	0.099	0.031	0.052
ITRS HP 2021	9.7	0.56	0.74	0.1	1,450	1.45 × 10^4	—	0.93	0.477	0.51
Scheme I	8.82	0.54	0.72	0.1	2,234	2.23 × 10^4	67.7	0.078	0.025	0.043
Scheme II	8.82	0.54	0.72	0.1	2,325	2.32 × 10^4	59.0	0.101	0.031	0.045
Scheme III	8.82	0.54	0.72	0.202	2,130	1.05 ×10^4	80.8	0.093	0.031	0.046
ITRS HP 2022	8.8	0.54	0.72	0.1	1,350	1.35 × 10^4	—	0.87	0.463	0.45
Scheme I	7.94	0.51	0.71	0.1	2,018	2.02 × 10^4	73.9	0.073	0.026	0.039
Scheme II	7.94	0.51	0.71	0.1	2,195	2.20 × 10^4	68.6	0.095	0.031	0.041
Scheme III	7.94	0.51	0.71	0.451	2,057	4.56 × 10^3	86.8	0.088	0.030	0.042
ITRS HP 2023	8.0	0.51	0.71	0.1	1,330	1.33 × 10^4	—	0.82	0.437	0.41
Scheme I	7.27	0.49	0.69	0.1	1,672	1.67 ×10^4	83.2	0.069	0.028	0.034
Scheme II	7.27	0.49	0.69	0.1	1,967	1.97 × 10^4	76.3	0.088	0.031	0.036
Scheme III	7.27	0.49	0.69	0.780	1,850	2.37 × 10^3	95.6	0.072	0.027	0.038
ITRS HP 2024	7.3	0.49	0.69	0.1	1,170	1.17 × 10^4	—	0.77	0.451	0.36
Scheme I	6.61	0.47	0.68	0.190	1,533	8.07 × 10^4	99.6	0.060	0.027	0.030
Scheme II	6.61	0.47	0.68	0.1	1,762	1.76 × 10^4	83.4	0.070	0.027	0.032
ITRS HP 2025	6.7	0.47	0.68	0.1	1,100	1.10 × 10^4	—	0.72	0.446	0.33
Scheme II	6.17	0.45	0.66	0.133	1,574	1.18 × 10^4	89.4	0.068	0.028	0.029
ITRS HP 2026	6.1	0.45	0.66	0.1	1,030	1.03 × 10^4	—	0.67	0.432	0.29

currents I_{min} (not off-state current, but the smallest current) are obtained at V_g = 0.8 V for all the DG ML BP TFETs, and we plot I_{min} as a function of the gate length L_g in Fig. 2(a). We obtain I_{min} values of 1.4 × 10^{-2}–1.9 × 10^{-1}, 3.1 × 10^{-2}–1.3 × 10^{-1}, and 1.4 × 10^{-1}–7.8 × 10^{-1} μA/μm for Schemes I–III, respectively, and I_{min} rapidly increases with the reduction in L_g in all the three schemes. The leakage currents satisfy the ITRS HP requirements (0.1 μA/μm) when L_g > 6.7 and 6.1 nm in the optimal Schemes I and II, respectively, but are still too high for the requirements of 2 × 10^{-5}–5 × 10^{-5} μA/μm for ITRS low-power devices.

Compared with our results, both I_{max} (1–200 μA/μm) and I_{min} (5 × 10^{-9}–3 × 10^{-5} μA/μm) of the DG ML BP TFETs with 10-nm-long gate at the tight binding level [14, 15] are much smaller. As the technical parameters (i.e., EOT and V_{ds}), doping concentration, band gap, and the theoretical level are all different, we perform a test and benchmark of I_{max} and I_{min} of our ML BP TFETs at the *ab initio* level against the ML/BL BP TFETs at the tight binding level in Table S1 in the ESM. In the test, we use the same technical parameters (EOT = 0.39 nm and V_{ds} = 0.5 V) and doping concentration (N_s/N_d = 5 × 10^{13}/–1 × 10^{13} cm^{-2}) as the work of Chang et al. [14]. Meanwhile, the band gaps are similar (0.88 eV (DFT) vs. 0.93 eV (TB)). We find I_{max} and I_{min} of ML BP TFET at the *ab initio* level

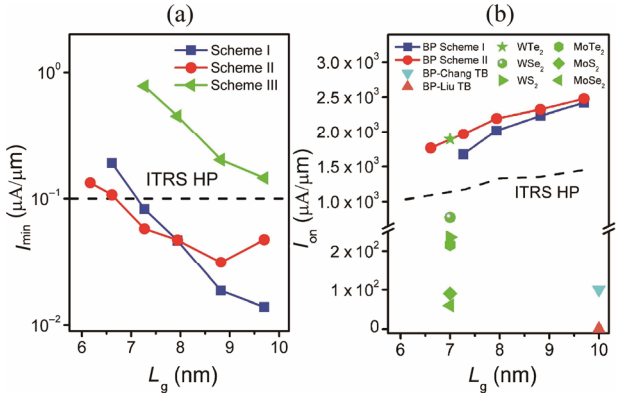

Figure 2 (a) I_{min} of the DG ML BP TFETs under the three schemes at the *ab initio* level against the ITRS goals (0.1 μA/μm) for the HP applications. (b) Benchmark of I_{on} of the DG ML BP TFETs under the two optimal schemes at the *ab initio* level against those of the DG ML BP TFETs [14, 15] at the tight binding level, DG ML TMD TFETs [34] at the *ab initio* level, and the ITRS requirements for HP devices. The transport directions of the ML BP are all along the armchair direction. All the off-states are set to 0.1 μA/μm.

are 3.5 × 10^3 and 7.6 × 10^{-4} μA/μm, respectively, which are both one order of magnitude larger than the values at the tight binding level of approximately 2 × 10^2 and 3 × 10^{-5} μA/μm, respectively. Such a discrepancy is attributed to the slightly larger effective mass and band gap (see Table S1 in the Electronic Supplementary material) at the *ab initio* level and the higher accuracy of *ab initio* theory itself.

The smallest values of I_{max} and I_{min} of approximately 1 and 5 × 10^{-9} μA/μm, respectively, obtained by Liu et al. [15] are due to the large quasi-particle gap (1.52 eV) adopted in the device simulation, as $T(E)$ has an exponential relation with E_g. We test the ML BP TFET with E_g = 1.52 eV at the quasi-particle level, and I_{max} and I_{min} are obtained as 4.8 × 10^2 and 3.8 × 10^{-7} μA/μm, respectively, which are approximately one order of magnitude and six orders of magnitude smaller than the values of 4.3 × 10^3 and 1.4 × 10^{-1} μA/μm at the DFT-GGA level (E_g = 0.88 eV), respectively. However, the observed transport band gap (1.0 eV) in ML BP SBFET [11] is much closer to the DFT-GGA value (0.88 eV) compared with the quasi-particle value (1.52 eV) obtained for the intrinsic ML BP. This can be attributed to the fact that many body effects have been significantly depressed in the FET configuration owing to the screening of the electron–electron interaction by doped carriers [27, 28]. Consequently, the quasi-particle band gap of an ML BP in the FET configuration is much smaller than that of an intrinsic ML BP but becomes quite close to the band gap at the DFT-GGA level of intrinsic ML BP.

We set the off-state currents I_{off} to 0.1 μA/μm according to the ITRS HP standard, and the on-state current (I_{on}) is obtained at a supply voltage (V_{dd}), where V_{dd} = |V_g (on) − V_g (off)| = V_{ds}. The on-state currents I_{on} are 1.7 × 10^3–2.4 × 10^3 μA/μm and 1.8 × 10^3–2.5 × 10^3 μA/μm in Schemes I and II for L_g = 7.27–9.70 nm and 6.67–9.70 nm, respectively. I_{on} monotonously increases with the increase in L_g. We benchmark I_{on} of DG ML BP TFETs against the DG ML BP TFETs obtained by Chang et al. [14] and Liu et al. [15] at the tight binding level, DG ML transition-metal dichalcogenide (TMD) TFETs at the *ab initio* level [34], and the ITRS requirements for HP devices in Fig. 2(b). Compared with the ML BP TFETs with L_g = 10 nm at the tight binding level, the obtained values of I_{on} are more than one and two orders of

magnitude larger than those of approximately 10^2 and 1 μA/μm obtained by Chang et al. [14] and Liu et al. [15] at a smaller $V_{ds} = V_{dd} = 0.5$ V, respectively. The remarkable discrepancy in I_{on} between the DFT and tight binding approximation is attributed to the inaccuracy of the tight binding method and the unoptimized doping concentration of previous works [14, 15]. Moreover, the extraordinarily small I_{on} (approximately 1 μA/μm) obtained by Liu et al. [15] originates from the adopted large band gap of 1.52 eV, which is overestimated in the FET configuration owing to the screening of the electron–electron interaction by doped carriers [27, 28]. Moreover, the I_{on} values of our ML BP TFETs with $L_g = 7$ nm are more than the values of 60–774 μA/μm of the examined ML TMD TFETs, except that of WTe_2 (1,890 μA/μm), by 2–33 times at the *ab initio* level, where the I_{on} values of the TMD TFETs are considered at V_{ds}/V_{dd} = 0.5/0.7 V with I_{off} considered as 4.7×10^{-4}–1.4×10^{-1} μA/μm [34]. Notably, the I_{on} values of our ML BP TFETs are prominently larger than the ITRS HP requirements by 43%–67% and 60%–72% in Schemes I and II, respectively.

The large on-state currents of our ML BP TFETs are attributed to the electronic nature of ML BP. In a TFET with a given L_g, the transmission coefficient $T(E) \propto e^{-\sqrt[4]{m_h m_e}\cdot\sqrt{E_g}}$, where m_h/m_e and E_g are the hole/electron effective mass along the transport direction and band gap, respectively. Thus, the very small value of m_h/m_e (0.14/0.14 m_0) in the armchair transport direction and the moderate value of E_g (0.9 eV) of ML BP result in the high on-state currents. Moreover, the anisotropic nature of ML BP is another key factor for the high on-state currents because $T(E)$ also depends on the projected density of states (PDOS) of the source/drain region (PDOS): $T(E) \propto$ PDOS (source) × PDOS (drain). PDOS (source/drain) depends on the hole/electron density of states (DOS) of the infinite ML BP, where DOS (source) = $\frac{g_S g_V}{2\pi\hbar^2}\sqrt{m_h^a m_h^z}$ and DOS (drain) = $\frac{g_S g_V}{2\pi\hbar^2}\sqrt{m_e^a m_e^z}$, where g_S and g_V represent the spin and valley degeneracies, respectively [35, 36]. As the effective masses along the armchair and zigzag directions are very light and heavy with m_h^a / m_e^a = 0.14/0.14 m_0 and m_h^z / m_e^z = 2.44/1.21 m_0, respectively, the product of m^a and m^z is, thus, a large number. Hence, the anisotropic nature of ML BP leads to a large DOS at the band edge, and thereupon leads to a large and steep PDOS (source/drain), which eventually results in a large $T(E)$ and current. We plot the PDOS of the source and drain and the transmission spectra $T(E)$ at $V_{ds} = 0.74$ V in Figs. 3(a) and 3(c), respectively. The band edges in the PDOS (source/drain) are large and steep, leading to large tunneling transmissions inside the bias window at on-state, as shown in Fig. 3(b).

In order to illustrate the gate control on the current, we plot the projected local density of states for the ML BP TFETs with $L_g = 9.70$ nm under the three schemes in Figs. 4(a)–4(f). In the bias window, the source valence bands and drain conduction bands overlap, which produces the BTBT currents. The small and large BTBT barrier widths correspond to the high ($V_g = 0.0$ V) (Figs. 4(a)–4(c)) and low (V_g = 0.8 V) current states (Figs. 4(d)–4(f)), respectively. We can observe that the leakage currents in both Schemes I and II are suppressed by the enhanced BTBT barrier width compared to Scheme III. The underlying mechanism of Scheme I is that the decrease in N_s reduces the overlapped region between the source valence and drain conduction bands, whereas the underlying mechanism of Scheme II is that the underlap structure increases the effective channel length. From Fig. 3(b), the tunneling $T(E)$ from the

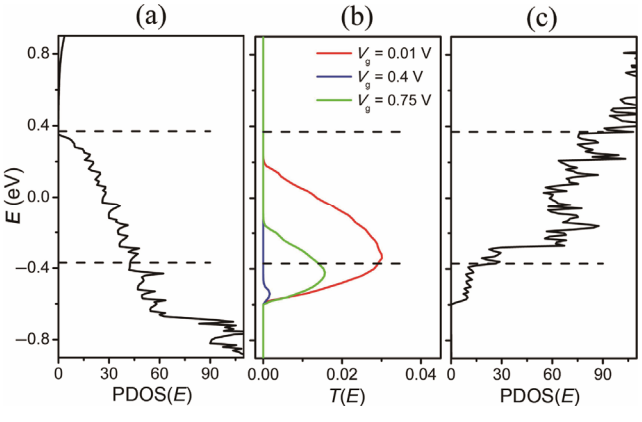

Figure 3 (a) Projected density of states (PDOS) of the source at $V_{ds} = 0.74$ V. (b) Transmission spectra for the 9.7-nm-gate-long DG ML BP TFET in Scheme I under on- ($V_g = 0.01$ V), intermediate ($V_g = 0.4$ V), and off- ($V_g = 0.75$ V) states. (c) PDOS of the drain at $V_{ds} = 0.74$ V. The black dash lines indicate the source-to-drain tunneling window of $V_{ds} = 0.74$ V.

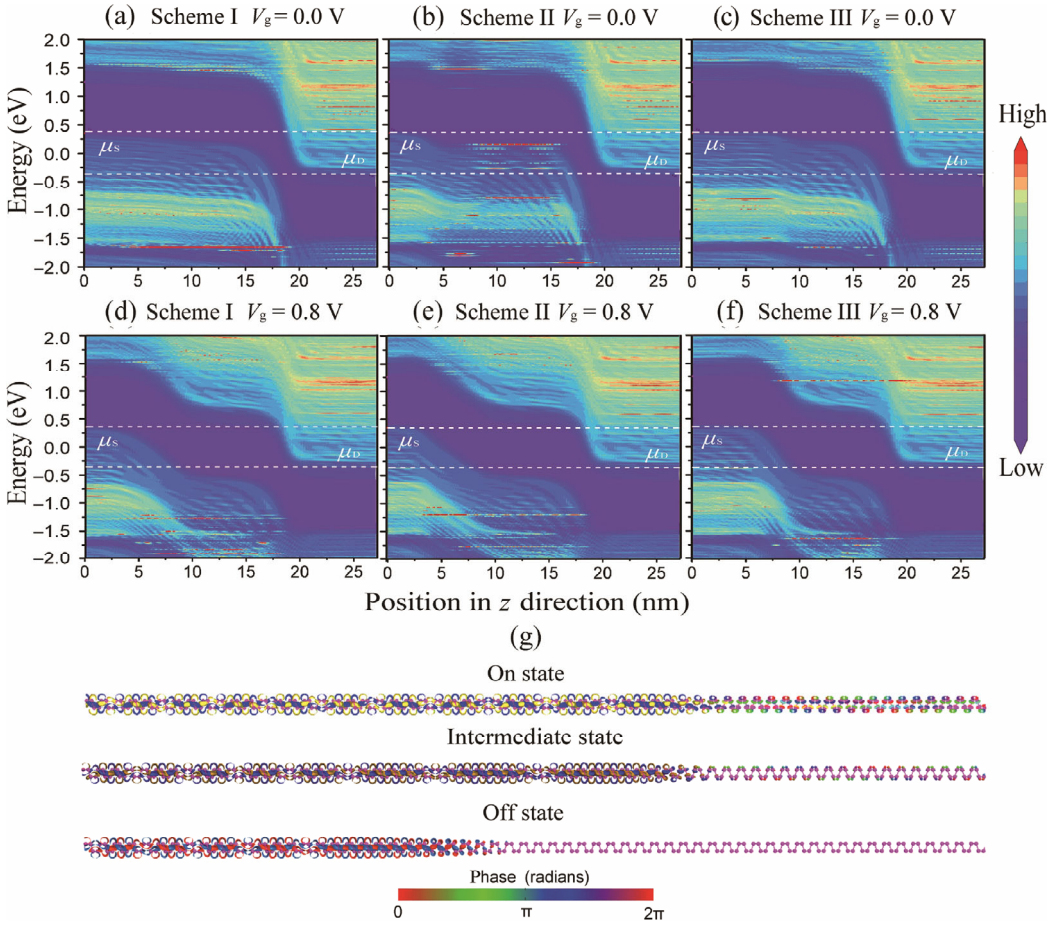

Figure 4 (a)–(f) Projected local density of states (L_g = 9.70 nm) at (a)–(c) V_g = 0.0 V and (d)–(f) V_g = 0.8 V under the three schemes. The white dash lines indicate the source-to-drain tunneling window of V_{ds} = 0.74 V. (g) Transmission eigenstates for the DG ML BP TFET with 9.7-nm-long gate in Scheme I at $E = -V_{ds}/2$ and Γ point under on- (V_g = 0.01 V), intermediate (V_g = 0.4 V), and off- (V_g = 0.75 V) states. The isovalue is 0.05 a.u.

source to drain is tuned by V_g, and we obtain large, medium, and small $T(E)$ in the bias window for V_g = 0.01 (at on-state), 0.4 (at intermediate state), and 0.75 V (at off-state), respectively. We also calculate the transmission eigenvalues and eigenstates for the DG ML BP TFET with 9.7-nm-long gate in Scheme I for $E = -V_{ds}/2$ and Γ points at V_g = 0.01, 0.4, and V_g = 0.75 V, respectively. The transmission eigenvalues decrease significantly from 1.61×10^{-1} at V_g = 0.01 V and 8.3×10^{-2} at V_g = 0.4 V to 9.76×10^{-6} at V_g = 0.75 V. The change of the transmission eigenstates is shown in Fig. 4(g), where the incoming electron wavefunction passes through the entire channel at V_g = 0.01 V and reaches the drain region, partially passes through the channel at V_g = 0.4 V, and is forbidden at V_g = 0.75 V.

SS is a key parameter of transistors, and it denotes the gate control ability at the subthreshold region. SS is defined as $SS = \frac{\partial V_g}{\partial \lg I_d}$, where I_d is the drain current. It indicates the gate voltage required to change the drain current by one order. The minimum SS is obtained at V_g = 0.7 V. We benchmark the minimum SS in the three schemes against those of the single-gated (SG) ML BP SBFETs [35], DG ML BP MOSFETs [37, 38], SG ML BP MOSFET [37], and DG ML MoS_2 SBFETs [39] in Fig. 5. The calculated SS of our ML BP TFETs monotonously decreases with the increase in L_g and can be arranged in the order of Schemes II < I < III with the values of 56–89, 74–96, and 58–100 mV/dec, respectively. Sub-60-mV/dec SS values are obtained for the ML BP TFETs with L_g = 9.7 and ≥ 8.8 nm in Schemes I and II, respectively. With similar L_g, the obtained SS values in Schemes I–II are much lower than the values of 83–121 and 63–87 mV/dec of

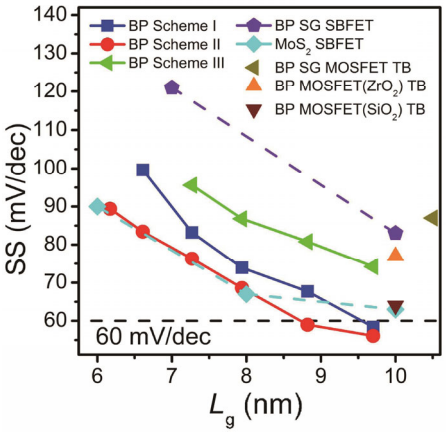

Figure 5 Benchmark of the minimum SS of the DG ML BP TFETs under the three schemes at the *ab initio* level against the SG ML BP SBFET with graphene electrode [35] at the *ab initio* level, DG ML BP MOSFET with ZrO_2 and SiO_2 gate dielectric [38] at the tight binding level, phonon-limited SG ML BP MOSFET [37] at the tight binding level, and DG ML MoS_2 SBFETs at the *ab initio* level [39]. The transport directions of the ML BP are all along the armchair direction.

their SBFET [35] and MOSFET [37, 38] counterparts, respectively. The obtained SS values in Schemes I and II are smaller than those of ML MoS_2 SBFETs [39] for $L_g > 9.2$ and 8 nm, respectively. The tunneling transport mechanism is responsible for the obtained small SS values, where the sub-60-mV/dec SS values break the Boltzmann thermal switching limit of conventional FETs. Moreover, the effective I_d of small SS can reach approximately 100 μA/μm, which is one and two orders of magnitude larger than that of the ML WTe_2 and MoS_2 TFETs with 7-nm-long gate [34] and significantly higher than that of the bulk TFETs at I_d = 10^{-7}–10^{-3} μA/μm [4].

The intrinsic gate capacitance (C_g) and delay time (τ) are two other major device figures of merit. The gate capacitance is calculated as $C_g = \frac{\partial Q_{ch}}{\partial V_g}$, where Q_{ch} is the total charge of the channel. A small value of C_g benefits rapid operation. We benchmark the calculated C_g in Scheme II against the ITRS requirements for HP devices and those of the DG ML BP SBFET [35] and DG ML MoS_2 SBFETs [39] in Fig. 6 (a). The calculated values of C_g increase with the increase in L_g and are 0.060–0.081, 0.068–0.106, and 0.072–0.099 fF/μm in Schemes I, II, and III, respectively, which are smaller than the ITRS values by approximately one order of magnitude. This is partly due to the presumption of ideal gates. The obtained values of τ are remarkably smaller than the values of 0.24–0.29 and 0.13–0.24 fF/μm of BP SBFETs and MoS_2 SBFETs with similar L_g, respectively.

Delay time is the duration for which the drain current lags behind the gate voltage, which is defined as $\tau = \frac{C_g V_{dd}}{I_{on}}$. It directly reflects the ability to handle a rapid operation. The small value of C_g and the large value of I_{on} result in a sufficiently small τ. We benchmark the calculated τ in Scheme II against the ITRS requirements for HP devices and those of the DG ML BP SBFETs [35], DG ML BP MOSFET [40], and DG ML MoS_2 SBFETs [39] in Fig. 6(b). The calculated values of τ are 0.025–0.027, 0.028–0.032, and 0.027–0.031 ps in Schemes I, II, and III, respectively, which are more than one order of magnitude smaller than the ITRS HP requirements of 0.432–0.477 ps. The calculated values of τ are comparable to their SBFET and MOSFET counterparts with similar L_g, with the values being slightly smaller than the values of 0.034–0.042 ps of their SBFET counterparts [35] and slightly larger than the value of 0.022 ps of their MOSFET counterpart [40]. The obtained values of τ are remarkably smaller than the values of 0.15–0.21 ps of MoS_2 SBFETs with similar L_g. This indicates the outstanding ability of fast switching of our DG ML

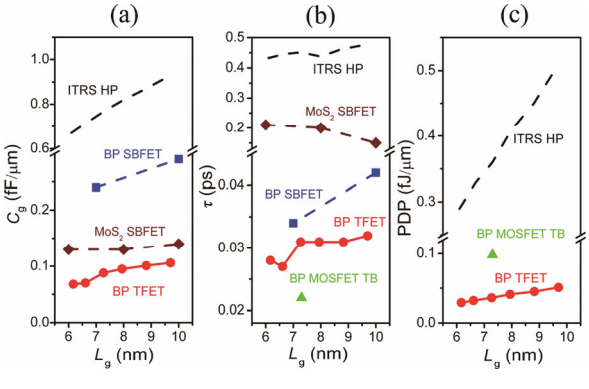

Figure 6 Benchmark of the (a) gate capacitance (C_g), (b) delay time (τ), and power dissipation (PDP) of the DG ML BP TFETs in Scheme II at the *ab initio* level against the ITRS 2013 requirements for HP devices, the ML BP DG SBFET with graphene electrode [35] at the *ab initio* level, ML BP DG MOSFET [40] at the tight binding level, and DG ML MoS_2 SBFETs at the *ab initio* level [39]. The transport directions are along the armchair direction

BP TFETs.

When considering very large-scale integration applications, power consumption is another major concern for FETs. We calculate the power dissipation (PDP) per width as $PDP = \frac{(Q_{on} - Q_{off}) \cdot V_{dd}}{W}$, where Q_{on} and Q_{off} are the total charges of the channel in the on- and off-states, respectively, and W is the channel width. We benchmark the calculated PDP in Scheme II against the ITRS requirements for HP devices, and those of the DG ML BP MOSFET [40] and DG ML MoS_2 SBFETs [39] in Fig. 6(c). The calculated PDP values slightly increase with the increase in gate length and are 0.030–0.050, 0.029–0.051, and 0.038–0.052 fJ/μm in Schemes I, II, and III, respectively, which are one order of magnitude smaller than the ITRS requirements of 0.29–0.51 fJ/μm and only one-third of the value of 0.098 fJ/μm of their MOSFET counterpart with similar L_g [40]. Apparently, our devices require less switching energy during the fast switching.

For practical applications of this ML BP TFET, synthesizing, scaling, and doping ways are three key factors. ML BP has been achieved successfully using mechanical exfoliation [12, 13]. Other techniques such as liquid exfoliation [41, 42], pulsed laser deposition [43], and plasma thinning [44] have been demonstrated to fabricate few-layer BPs. Moreover, the recent development of high quality and purity orthorhombic black phosphors from red phosphorus facilitates economic and large-scale preparation of ML BP [45]. Scaling the channel to sub-10-nm patterning resolution is the second important issue for practical device application. An experimental breakthrough of the sub-10-nm ML MoS_2 FETs [16–19] is obtained via directed self-assembly of block copolymers, hydrogen plasma etching of graphene electrodes plus transferring the 2D channel, corrosion cracking with the assistance of a cleavage plane of the bismuth trioxide, and utilizing the natural dimensions of a carbon nanotube. The same technologies could be applied to fabricate of the sub-10-nm ML BP TFETs.

Doping regions for electrodes is another key technology. The conventional state-of-the-art substitutional doping strategy for bulk semiconductors is not practical for 2D materials. High- or low-work-function metal electrode contacts are inappropriate for the fabrication of BP TFETs because such metal–semiconductor contacts destroy the electronic structure of BP [29–31]. Experimentally, surface charge transfer doping [46, 47], bulk doping [48, 49], and electrostatic doping [50, 51] techniques have been utilized to dope BP. The most feasible way to fabricate a BP TFET is the electrostatic gating technique as it can inject electrons or holes into the respective bands with controllable doping levels. Using the practical synthesis, scaling, and doping schemes, the fabrication of ML BP TFETs is foreseeable as long as there is sufficient research interest in this topic

4 Conclusions

In summary, we examined the ML BP TFETs along the armchair directions for possible HP applications at the sub-10-nm scale using the rigorous *ab initio* quantum transport simulations. Under the optimal schemes, the on-state currents exceeded the ITRS goals by 39%–72% for the HP applications for $L_g \geq 6.7$ nm, and the delay time and power dissipation surpassed the ITRS HP transistor requirement by one order of magnitude. Sub-60-mV/dec subthreshold swing was also achieved, which is much lower than that of their SBFET and MOSFET counterparts. Our study is expected to encourage future experimental investigations on the sub-10-nm TFETs based on ML BP.

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Electronic Supplementary Material: Supplementary material (benchmark of I_{max} and I_{min} of the ML BP TFETs at the *ab initio* level against those of the ML/BL BP TFETs at the tight binding level; convergence test of the basis set; benchmark of the calculated transfer characteristic against the experimental one for the

MoS_2 FET with 1-nm-long gate; device performance of the ML BP TFETs as a function of the source and drain doping level and the underlap region; and device transfer characteristics of the ML BP TFETs at opposite source/ drain doping levels) is available in the online version of this article at https://doi.org/10.1007/s12274-017-1895-6.

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